General Description

Renesas SLG4E46882 is a low power and small form device. The SoC is housed in a 1mm x 1.2mm STQFN package which is optimal for using with small devices.

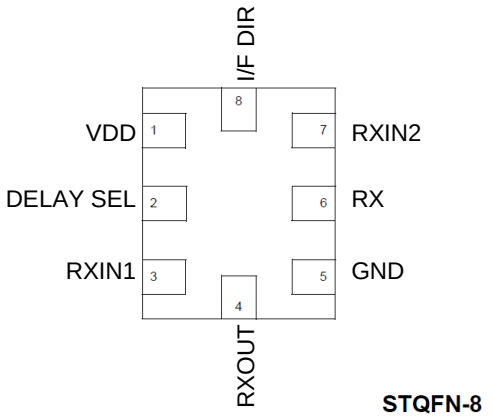
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 8 Package

Output Summary

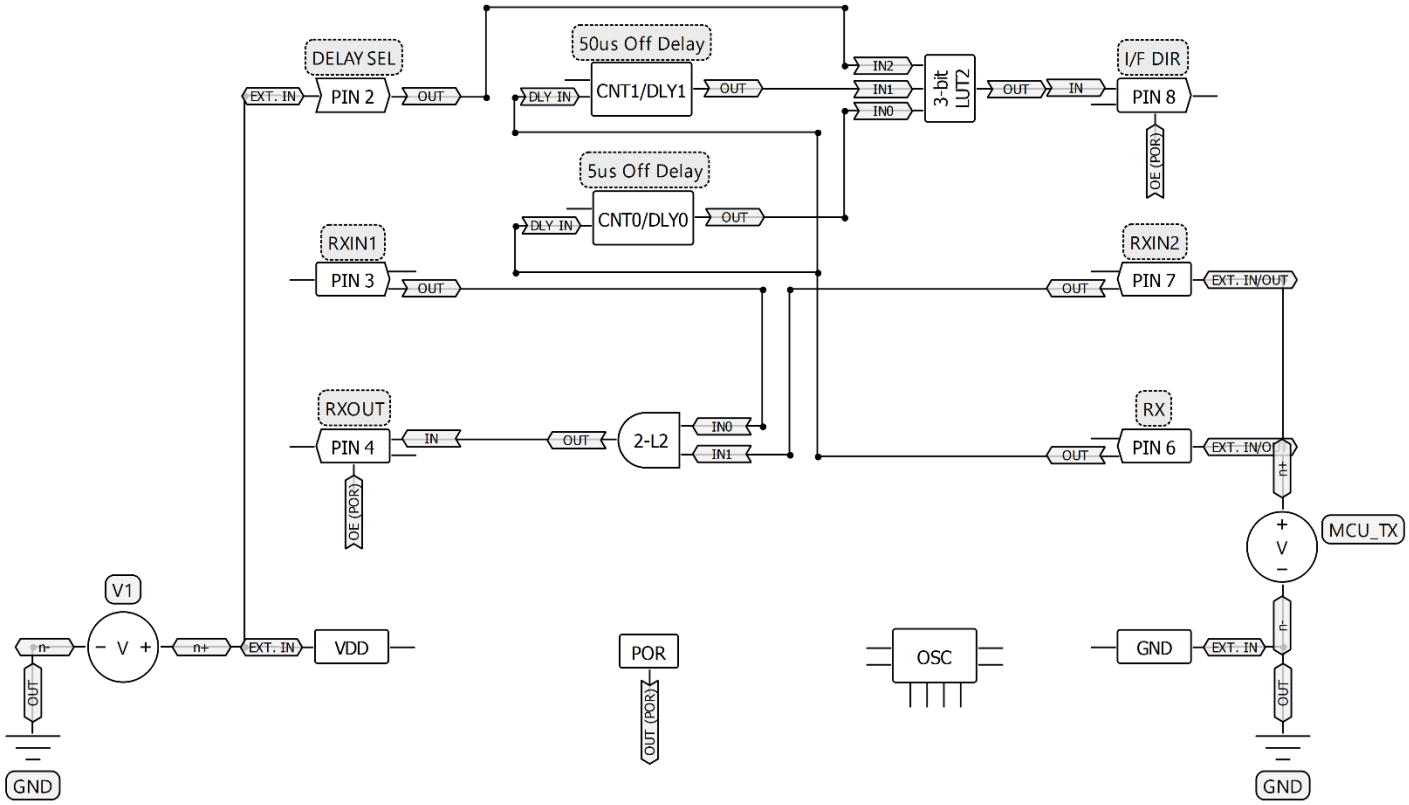
1 Output - Push Pull 1X
1 Output - Push Pull 2X

Pin Configuration



STQFN-8
(Top View)

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	DELAY SEL	Digital Input	Digital Input without Schmitt trigger	100kΩ pulldown
3	RXIN1	Digital Input	Digital Input with Schmitt trigger	10kΩ pullup
4	RXOUT	Digital Output	Push Pull 2X	floating
5	GND	GND	Ground	--
6	RX	Digital Input	Digital Input with Schmitt trigger	100kΩ pullup
7	RXIN2	Digital Input	Digital Input with Schmitt trigger	10kΩ pullup
8	I/F DIR	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG4E46882V	8-pin STQFN
SLG4E46882V	8-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	° C
Junction Temperature		--	150	° C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.8	3.3	5.2	V
T_A	Operating Temperature		-20	25	70	° C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1.6	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=1.8V	1.071	--	VDD	V
		Logic Input at VDD=3.3V	1.84	--	VDD	V
		Logic Input at VDD=5.0V	2.744	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=1.8V	1.276	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=3.3V	2.17	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=5.0V	3.19	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=1.8V	0	--	0.73	V
		Logic Input at VDD=3.3V	0	--	1.255	V
		Logic Input at VDD=5.0V	0	--	1.877	V
		Logic Input with Schmitt Trigger at VDD=1.8V	0	--	0.475	V
		Logic Input with Schmitt Trigger at VDD=3.3V	0	--	0.934	V
		Logic Input with Schmitt Trigger at VDD=5.0V	0	--	1.488	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=100µA, at VDD=1.8V	1.692	1.788	--	V

		Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=3mA, at VDD=3.3V	2.721	3.108	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=5mA, at VDD=5.0V	4.171	4.761	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=100µA, at VDD=1.8V	1.7	1.794	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=3mA, at VDD=3.3V	2.864	3.204	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=5mA, at VDD=5.0V	4.336	4.879	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=100µA, at VDD=1.8V	--	0.01	0.016	V
		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	0.175	0.257	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	0.225	0.325	V
		Push-Pull 2X, I_{OL}=100µA, at VDD=1.8V	--	0.005	0.007	V
		Push-Pull 2X, I_{OL}=3mA, at VDD=3.3V	--	0.086	0.122	V
		Push-Pull 2X, I_{OL}=5mA, at VDD=5.0V	--	0.111	0.156	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=VDD-0.2V, at VDD=1.8V	1.045	1.506	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=2.4V, at VDD=3.3V	5.774	11.066	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=2.4V, at VDD=5.0V	20.656	30.203	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=VDD-0.2V, at VDD=1.8V	2.097	2.982	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=3.3V	11.351	21.73	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=5.0V	40.17	56.319	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=1.8V	0.984	1.363	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.491	6.438	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	6.087	8.611	--	mA
		Push-Pull 2X, V_{OL}=0.15V, at VDD=1.8V	2.011	2.743	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=3.3V	9.124	12.884	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=5.0V	12.321	17.147	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 3, 7	--	10	--	kΩ
		Pull up on PIN 6	--	100	--	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	--	100	--	kΩ
T_{DLY0}	Delay0 Time	At temperature 25°C	3.64	5.12	6.44	µs
		At temperature -20 +70°C (Note 3)	3.64	5.14	6.5	µs
T_{DLY1}	Delay1 Time	At temperature 25°C	43.24	50.12	52.94	µs
		At temperature -20 +70°C (Note 3)	42.9	50.14	55.28	µs
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	0.54	--	ms

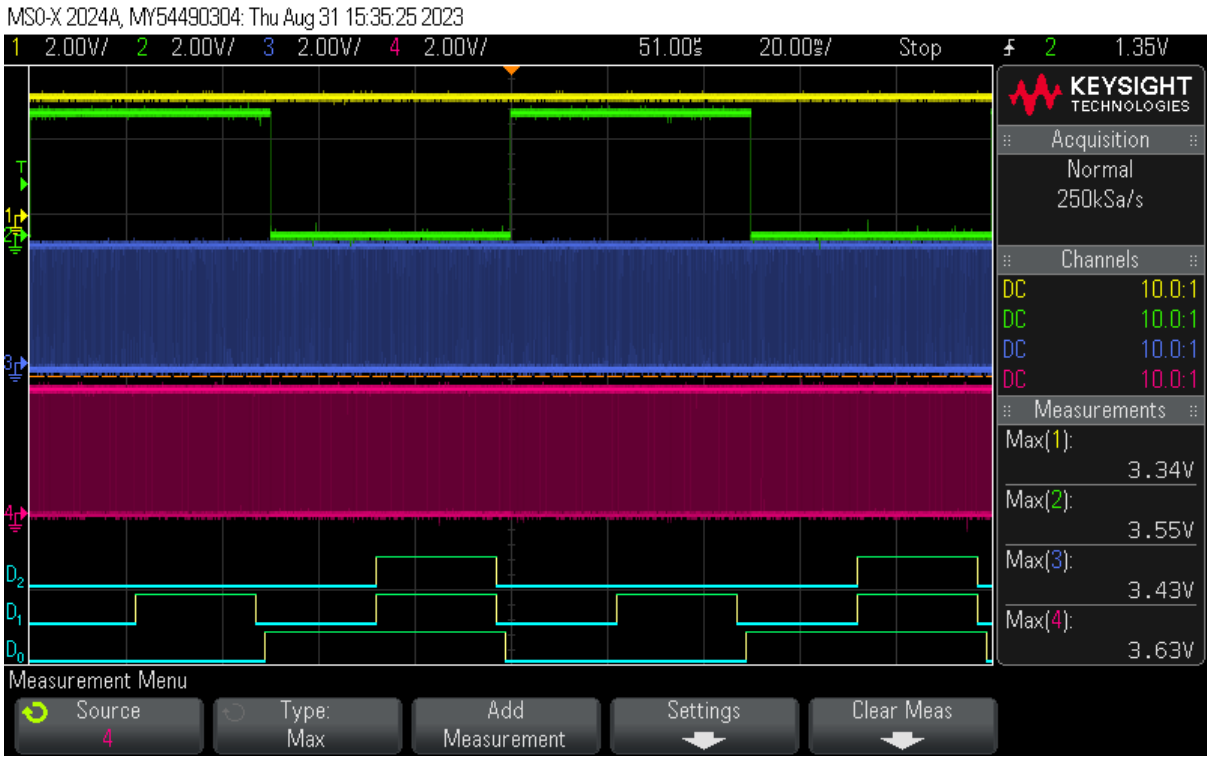
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.303	1.506	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.675	0.901	1.174	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.
3. Guaranteed by Design.

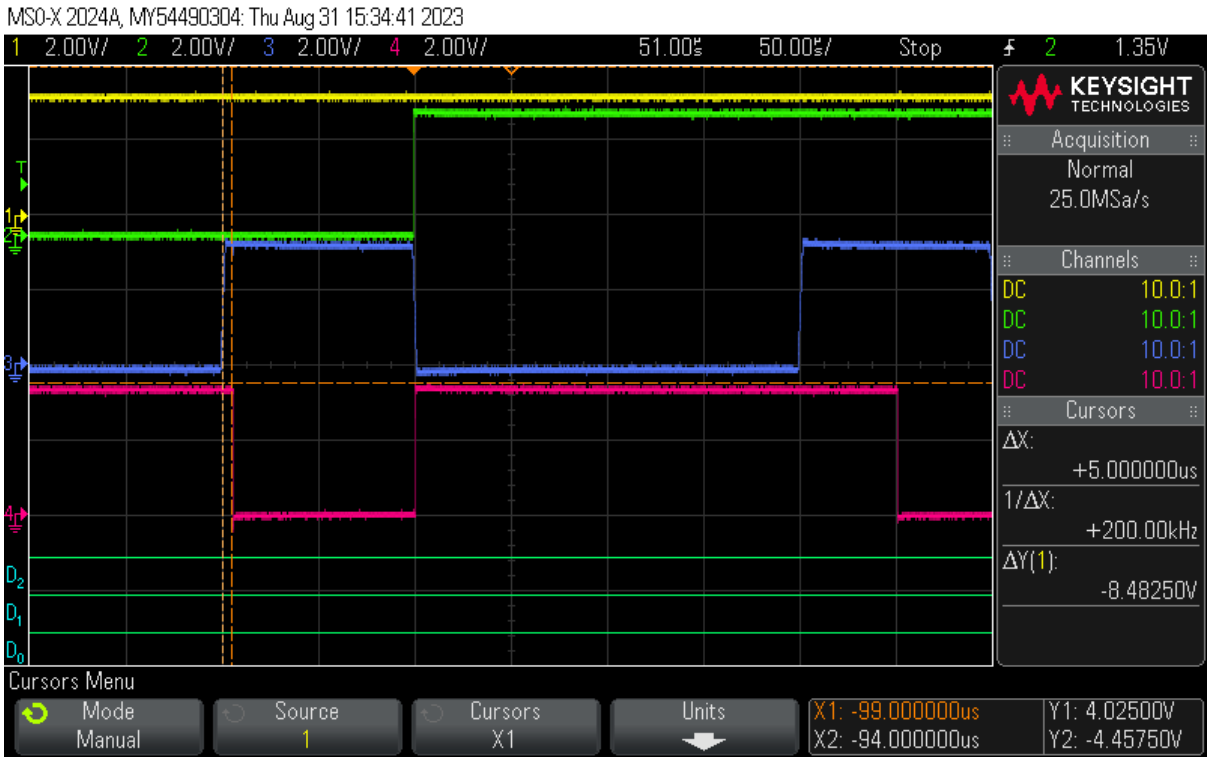
Functionality Waveforms

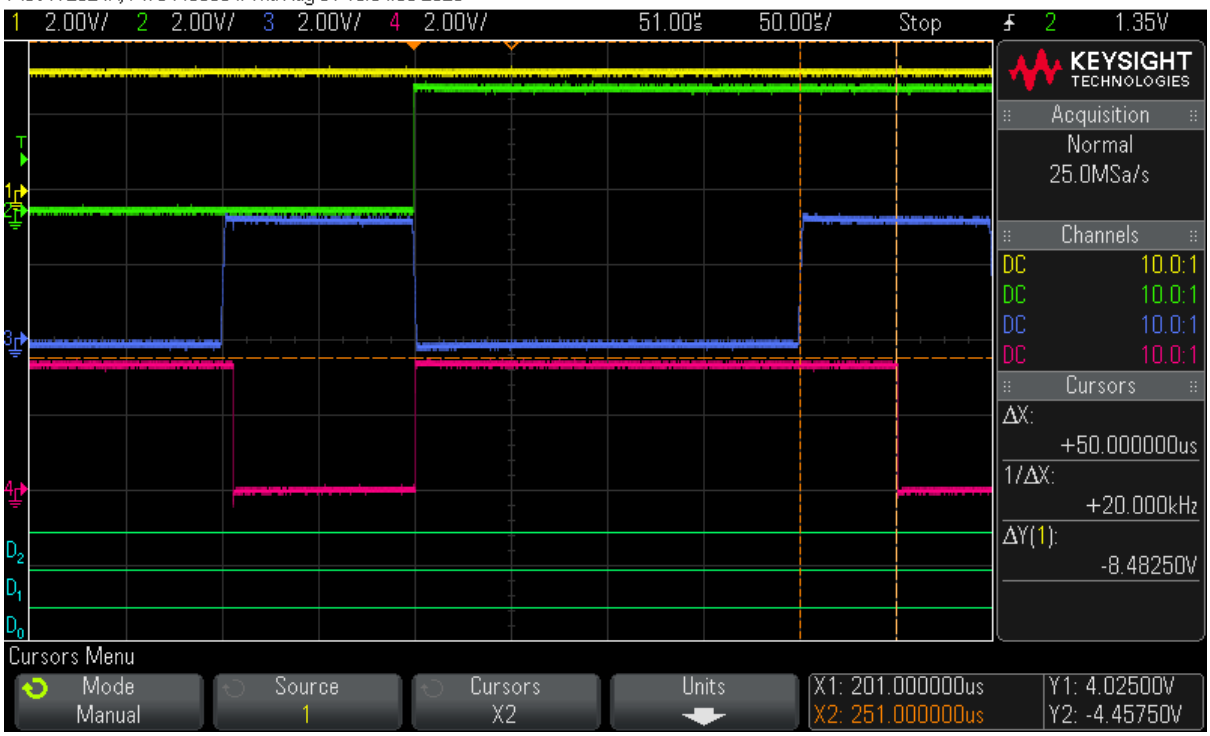
Channel 1 (yellow/top line) – PIN# 1 (VDD)
Channel 2 (green/2nd line) – PIN# 2 (DELAY SEL)
Channel 3 (blue/3rd line) – PIN# 6 (RX)
Channel 4 (magenta/bottom line) – PIN# 8 (I/F DIR)
D0 – PIN# 3 (RXIN1)
D1 – PIN# 7 (RXIN2)
D2 – PIN# 4 (RXOUT)

1. Overall view

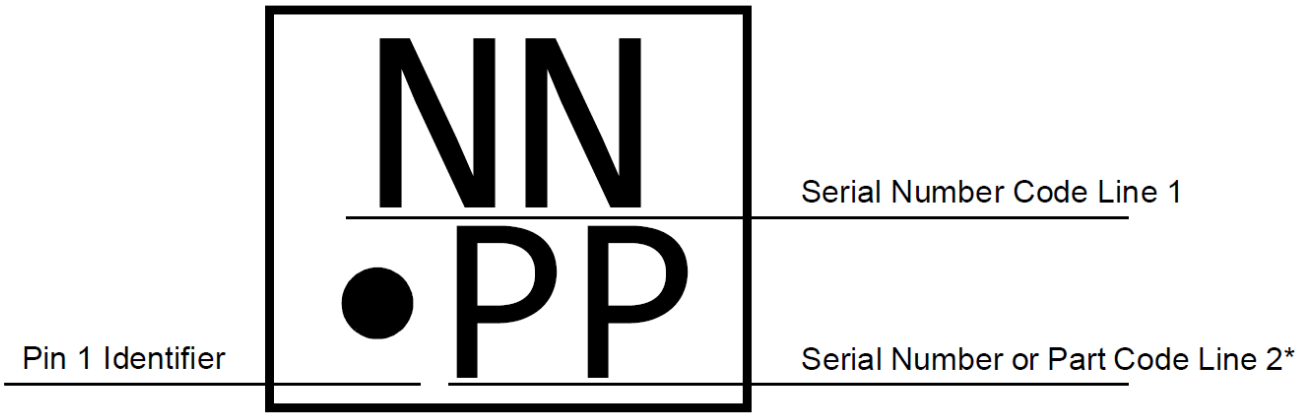


2. Details show





Package Top Marking



* PP may consist of the special characters +, -, and = for a total of 9 different combinations, or may consist of two character alphanumeric Part Code (A-Z and 0-9), depending on time of marking.

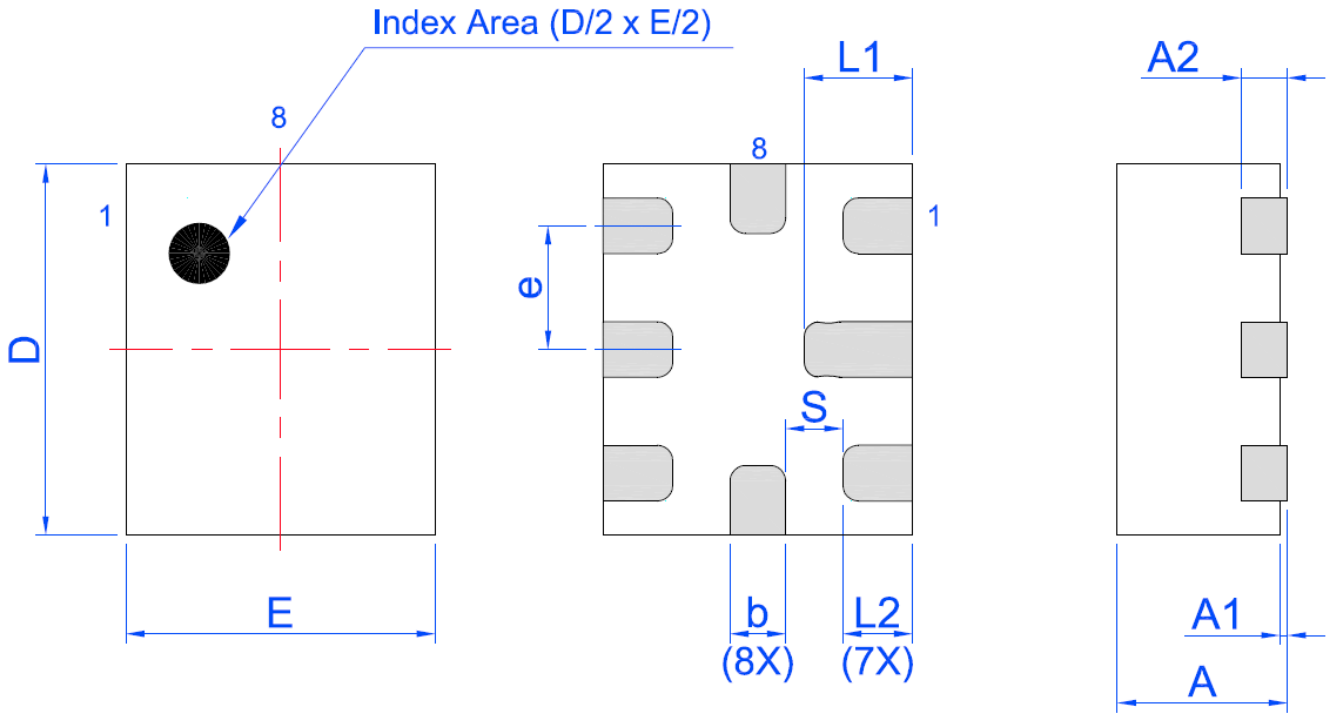
Note: The SN Code (Line 1 and Line 2) is generated during production, and encodes information including part number, programming code number, date code and lot code. This same information is provided in plain text form on a label placed on the reel. If you need assistance in decoding the SN Code, please contact Dialog Semiconductor.

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	U	0xAA67673E			08/31/2023

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

8 Lead STQFN Package 1.0 x 1.2 mm



TOP View **BTM View** **SIDE View**

Unit: mm

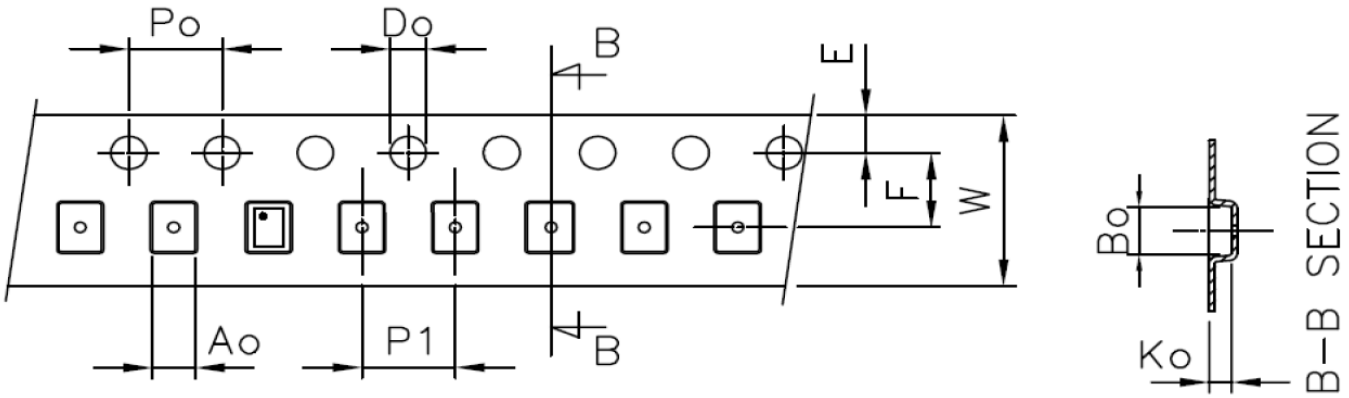
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.15	1.20	1.25
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L1	0.30	0.35	0.40
b	0.13	0.18	0.23	L2	0.175	0.225	0.275
e	0.40 BSC			S	0.185 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 8L 0.4P FC Green	8	1.0x1.2x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 8L 0.4P FC Green	1.16	1.38	0.71	4	4	1.5	1.75	3.5	8



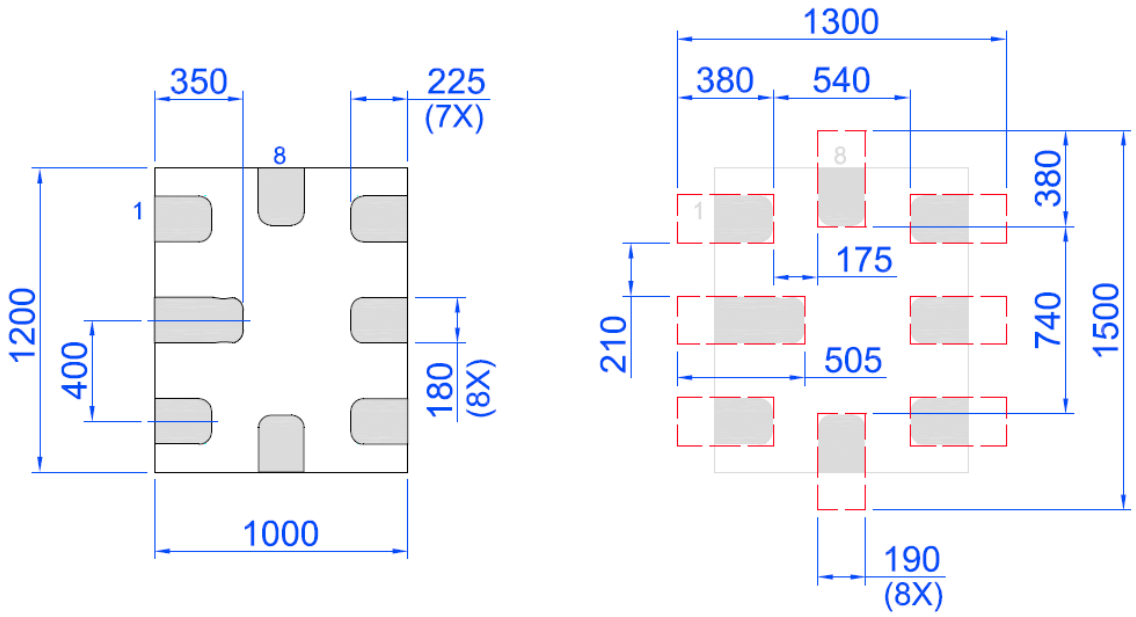
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.66 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(PKG face down)

Recommended Landing Pattern
(PKG face down)



Unit: um

Datasheet Revision History

Date	Version	Change
08/31/2023	0.10	New design for SLG46108 chip